A Diophantine Frequency Synthesizer for the Examination of High Spectral Purity

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Abstract—**Diophantine Frequency Synthesis (DFS), a number theoretic approach to the design of very high resolution and agile frequency synthesizers was introduced at the IEEE Frequency Control Symposium of 2006, [1]. Since DFS uses frequency addition (and/or subtraction), concerns for the impact of mixing spurs in the spectral purity was raised.**

Further work has been performed to address this issue and is reported in this paper. The focus has been on basic DFS architecture targeting micro-phase type applications. The design goal has been to achieve 100 dB spurious free dynamic range (SPFD) with minimal circuit complexity.

The results of the examination demonstrate that the use of DFS does not impart any extraordinary design constraints to spectral purity from that of other topology choices. In fact, the flexibility of the design technique from its applied math basis allows this demonstration synthesizer to be realized with simple and expedient construction.

I. Introduction

Frequency synthesizers are essential elements to modern navigation and communication systems, as they provide the means to align and synchronize distributed transmitters and receivers with high signal purity. The degree of synchronization and signal purity is directly proportional to the quality of service offered by optical data networks and wireless communications. When the quality of service is compromised, the economic return of the transmission infrastructure cannot be optimized.

The previous art in frequency synthesizer design requires undesirable trade-offs among these four essential aspects:

Range—the magnitude of output frequency variation

Resolution—the accuracy to which the synthesized frequency can be aligned to the desired channel

Agility—the speed required for the synthesizer to change from one frequency to the next

Spectral Purity—the fidelity of the output tone in both noise and unwanted spurious tones.

In 2006, a novel approach, known as Diophantine Frequency Synthesis (DFS) [1,5], was introduced which we believe alleviates the conventional trades in performance for frequency synthesizer design without significantly taxing system complexity or resources. Our motivation for this paper emerged from collegial exchange in reference to the claim that DFS should provide high spectral purity, even in synthesizers with much less than 0.1 PPM resolution steps, because of its design property of allowing phase-comparator frequencies orders of magnitude higher than resolution. In general, we make this claim in comparison with other fine frequency synthesizer methods such as direct digital synthesis (DDS) or fractional-N modulators which are known to present a high degree of unwanted spurious into the output spectrum through the fundamental process they impart on the input reference signal [2].

DFS uses only exactly-periodic signals, without employing dithering, interpolation, pulse removal or any other approximately-periodic waveform that may corrupt the near-in spectrum. Our purpose here is to show that high spectral purity can be achieved in a practical, high frequency resolution DFS demonstration synthesizer since it presents no discontinuity of the reference frequency phase, such as DDS or fractional-N, and unlike these methods, DFS does not require any special devices such as high resolution digital to analog converters, accumulators, sigma-delta modulator to control the spurious level of the output signal. Since simulation of spectral purity is difficult, we pursued a physical demonstration.

However, like multiple loop PLL synthesizer architectures, DFS does require mixing (or multiplication) to achieve the output signal. This means that DFS synthesizers may suffer from unwanted spurious if attention to the circuit design is not adequately respected. Our design goal of high spectral purity with less than -100 dBc spurious free dynamic range (SPFD)

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is a significant challenge to any synthesizer approach and our desire is to show that DFS presents no unique design related constraints. Rather DFS' flexibility gives an advantage to achieving this level of performance in fine step resolution frequency synthesis.

II. DFS – ELEMENTS OF THE THEORY

DFS is a number-theoretic approach to frequency synthesis based on mathematical properties of integer numbers and linear Diophantine equations [5]. (By definition, a Diophantine equation is an algebraic equation whose solutions are required to be integers) [4].

DFS results in high-level architectures using two or more individual PLLs. It distributes the desired output frequency resolution among these constituent PLLs in such a manner that the resultant output fractional-frequency resolution **is equal to the product** of the constituent PLLs' fractional-frequency resolutions. Consequently, this property of DFS allows for the output frequency step to be made (arbitrarily) small without using large prescalers, (N_i's), or small PLL reference frequencies $(m_i/N_i)f_{in}$. These are illustrated in the following examples.

A. Fundamental Concepts of DFS

DFS considers a PLL as a multiplier of the input frequency f_{in} by a rational number m_i/N_i, as shown in Fig.1.

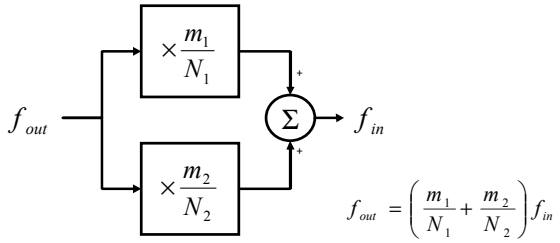

Figure 1. Two PLL DFS architecture

The sum or differences of the PLL-output frequencies f_1, f_2 can be generated by appropriate mixing, or more involved Cartesian multiplication etc, to produce the output signal f_{out}.

Note that the frequency resolution of the **individual** PLLs in Fig. 1 equals PLL's phase-comparator frequency f_{in}/N_i. This means that to achieve smaller frequency steps (higher resolution) from a single PLL, a larger prescaler N_i, and/or smaller f_{in} are needed. This, necessarily results in a smaller phase-comparator frequency implying slowed frequency lock acquisition (agility) and increased spurious signals levels and tones closer to the carrier signal of f_{out} [3].

DFS overcomes these problems as it allows for both large phase-comparator frequency at each constituent PLL and small frequency step resolution at the output of the synthesizer, e.g. equal to $f_{in}/(N_1 N_2)$ in Fig. 1.

Note that throughout this paper the prescalers (N_i's), of the PLLs are assumed to have a fixed size. Moreover, the greatest common divisor of every pair (N_i, N_j) is 1. This is a requirement of DFS. We also partition the feedback divider m_k into a sum of a fixed value $\overline{m}_k$ and a variable part which ranges from $-N_k$ to N_k. So $m_k : \overline{m}_k - N_k, \ldots, \overline{m}_k + N_k$.

The following example clarifies the previous definitions. The general theory of DFS can be found in [5].

B. Example of DFS in the Two PLL Case

Consider the DFS architecture of Fig. 2 consisting of two PLLs whose output frequencies are summed resulting in f_{out} given by (2) below.

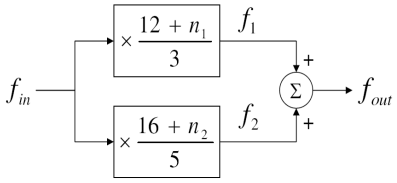

Figure 2. A simple two-PLL DFS scheme (borrowed from [5]).

$$f_{out} = \left(\frac{12+n_1}{3} + \frac{16+n_2}{5}\right) f_{in} \tag{2}$$

Following the concepts of DFS [5], the prescalers are $N_1 = 3$ and $N_2 = 5$, both fixed and relatively prime. The feedback dividers $12 + n_1$ and $16 + n_2$ are such that $-3 \le n_1 \le 3$ and $-5 \le n_2 \le 5$. So, the range of each PLL feedback divider is twice the size of the corresponding prescaler.

Frequency f_1 can take any of seven values:

$$f_1 \in \left\{\frac{9}{3}, \frac{10}{3}, \ldots, \frac{15}{3}\right\} \tag{3}$$

and in a similar manner f_1 can be any of eleven values.

$$f_2 \in \left\{\frac{11}{5}, \frac{12}{5}, \ldots, \frac{21}{5}\right\}$$

Table I (borrowed from [1]) shows the range of possible output frequencies f_{out} that can be generated using the DFS algorithm (to program the values of n_1 and n_2 within their specified ranges). They satisfy

$$\frac{n_1}{3} + \frac{n_2}{5} = \frac{a}{15} \tag{4}$$

Specifically, we can synthesize all frequencies of the form,

$$f_{out} = \overline{f_{out}} + \frac{a}{15} \tag{5}$$

with the variable a taking the values -15,-14,-13,…, 14, 15, and the central frequency being

$$f_{out} = \frac{108}{15} f_{in}.$$

In contrast, the phase comparator frequencies of the individual PLLs are at least 9/3 fin or 11/5 fin with a synthesizer frequency resolution step size of 1/15.

Taking this two PLL example generally, we can state that DFS develops,

$$f_{out} = \left(\frac{\overline{m}_1}{N_1} + \frac{\overline{m}_2}{N_2}\right) f_{in} + \left(\frac{a}{N_1 N_2}\right) f_{in} \tag{6}$$

where the variable part containing a can take any of the consecutive values $-N_1N_2, \ldots N_1N_2$. This leads by inspection of (6) to the fundamental property of DFS that the frequency resolution step can be much smaller than the phase comparator frequencies of each PLL.

$$\frac{f_{in}}{N_1 N_2} << \frac{f_{in}}{N_1}, \frac{f_{in}}{N_2} \tag{7}$$

The relation between n1, n2 and a is non-trivial and in same cases is not unique. However, it is proven in [5] that if we have the solution for a = 1, we can very easily generate solutions for every other value of a; therefore, very few numbers have to be stored. A detailed description of how to solve linear Diophantine equations efficiently is also available in [5].

C. *Frequency Mixing - Notation*

Mixing of two signals at frequencies $f1$ and $f2$ is denoted as in Fig. 3, the outcome can be chosen to be either $f1 + f2$ or $f1 - f2$. The choice of the sum or the difference dictates only the central frequency of the phase comparator frequency and not the resolution or the range of the DFS synthesizer. Mixing of three or more signals has a similar interpretation. Note that the order of performing the mixing of the signals may be important for getting a spectrally pure output signal.

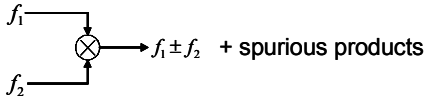

Figure 3. Mixing diagram in the context of DFS

Minimization of mixing spurs involves the choice of the central frequencies of the phase comparators and frequency ranges of the mixed signals, the choice of the sum or difference of their frequencies and of course the type of the mixer. The example that follows provide some indications regarding these choices, however, the goal of this section is only to lay out the principles of DFS required to understand the circuit topology of the demonstration synthesizer, discussed later.

TABLE I. FOUT SYNTHESIZED BY THE DFS OF FIG. 3 ([1])

$$f_{out} = \left(\frac{n_1}{3} + \frac{n_2}{5} + \frac{12}{3} + \frac{16}{5}\right) f_{in}$$

n_1	n_2	$\frac{f_{out}}{f_{in}}$	=	$\left(\frac{n_1}{3} + \frac{n_2}{5}\right)$	+	$\left(\frac{12}{3} + \frac{16}{5}\right)$
-3	0	93/15	=	-15/15	+	108/15
-1	-3	94/15	=	-14/15	+	108/15
-2	-1	95/15	=	-13/15	+	108/15
-3	1	96/15	=	-12/15	+	108/15
-1	-2	97/15	=	-11/15	+	108/15
-2	0	98/15	=	-10/15	+	108/15
-3	2	99/15	=	-9/15	+	108/15
-1	-1	100/15	=	-8/15	+	108/15
-2	1	101/15	=	-7/15	+	108/15
-3	3	102/15	=	-6/15	+	108/15
-1	0	103/15	=	-5/15	+	108/15
-2	2	104/15	=	-4/15	+	108/15
-3	4	105/15	=	-3/15	+	108/15
-1	1	106/15	=	-2/15	+	108/15
-2	3	107/15	=	-1/15	+	108/15
0	0	108/15	=	0/15	+	108/15
-1	2	109/15	=	1/15	+	108/15
-2	4	110/15	=	2/15	+	108/15
0	1	111/15	=	3/15	+	108/15
-1	3	112/15	=	4/15	+	108/15
1	0	113/15	=	5/15	+	108/15
0	2	114/15	=	6/15	+	108/15
-1	4	115/15	=	7/15	+	108/15
1	1	116/15	=	8/15	+	108/15
0	3	117/15	=	9/15	+	108/15
2	0	118/15	=	10/15	+	108/15
1	2	119/15	=	11/15	+	108/15
0	4	120/15	=	12/15	+	108/15
2	1	121/15	=	13/15	+	108/15
1	3	122/15	=	14/15	+	108/15
3	0	123/15	=	15/15	+	108/15

III. DESIGN CONSIDERATIONS FOR HIGH SPECTRAL PURITY DFS DEMONSTRATION

The DFS theory and solution strategy for high resolution synthesizers has been well developed and demonstrated. However simulation of spectral purity is difficult and so we pursued a practical demonstration circuit. Our design goal of high spectral purity with a spurious free dynamic range < -100 dBc is a significant challenge to any synthesizer approach and our desire is to show that DFS presents no unique design related constraints. Rather its flexibility and that DFS can be implemented with simple well chosen devices and circuit topologies give an advantage to achieving this performance.

Our selection for an appropriate DFS realization of very fine frequency resolution synthesizer with high spectral purity is motivated by very important applications in frequency alignment/translation circuits for synchronous distributed communication systems, maintenance of autonomous clock holdover and micro-phase steppers in laboratory timekeeping systems. In all of these applications, a local system frequency and/or phase must be generated and maintained to a very high degree of accuracy in reference to a global source, i.e. E1/T1 in wireless cellular telephony or STM-1 in Synchronous Digital Hierarchy (SDH). Systems for equipment in these

applications also require good spectral purity as unwanted spurious and noise corrupt data and limit bandwidth utilization. In frequency synthesizers for these systems, designers must carefully consider signal purity, resolution (accuracy to the global reference) and complexity against economic cost of the system. The introduction of DDS and fractional-N synthesis design techniques has been widely adopted for these systems as high frequency resolution (accuracy) and fast acquisition (settling time) can be achieved without the complexity of traditional multiple loop synthesizers. DDS and fractional-N architectures also promote the use micro-circuits and integration.

However DDS and fractional-N both cause phase perturbations in their basic operation schemes leading to coherent spurious generation. In the case of DDS, accuracy to a desired frequency is necessarily compromised by the incidence of truncation spurious attributable to the finite size of the DAC [3]. Our approach was to build a very high resolution, small frequency offset VHF synthesizer from DFS to allow very fine frequency adjustment of a fixed, input reference signal. DFS itself is not inherently phase perturbing like DDS or fractional N, so high spectral purity is a function of the k-order of the design topology and our choice for the solution for $\overline{m}_1 \ldots \overline{m}_k$ and a as described in the preceding sections. Most importantly, our demonstration synthesizer placed high attention in circuit design and our selection of critical devices; e.g. mixers, comparators and loop filters. We also emphasized the use of digital circuitry in the design to provide an easy path to possible small scale integration on-chip. The attempt was to create the demonstration with simple, all digital elements and expedient construction techniques.

A. Frequency Mixing

The key to low spurious production is the mixing method since DFS uses only periodic signals to generate its output and the mixer provides the only circuit element for non-linear signal production. Consequently, our first focus was placed on the mixing method as it determines the capability to meet our high spectral purity goals. We believed that if we got the mixing circuit design right, the balance of the circuitry would be less dominant.

Referring to Fig. 2, the unwanted mixing products, spurious, related to the IF (f1 ± f2) output can be proportionally suppressed as,

$$\frac{|f_1 - f_2|}{f_1 + f_2} << 1 \tag{8}$$

For example, using an exclusive OR gate for mixing of digital signals with f_1=1MHz and f_2=1MHz+10kHz theoretically results in -80dBc or better spurious free dynamic range (SPFD) in the span 0 Hz to 20 kHz. Likewise for D-Flip-Flop mixing of digital signals with f1=10MHz , f2=10MHz+1kHz, the SFDR also results in -80dBc or better in the span 0 Hz to 2 kHz. In this application of a VHF (~100 MHz) DFS synthesizer, we could keep the phase comparator signals (IF) in the kHz region, thereby permitting compliance to our SPFD goal of < -100db for either digital mixing choice without having the phase comparator signals also be so close to make loop filtering difficult.

B. Frequency Offsetting

Fig. 4 is convenient synthesizer architecture for deriving the sum or difference between a large *f*in and a small offset frequency (*f*). For use in our DFS demonstration, the phase comparator frequency from a DFS determined PLL will be used for the offset frequency (*f*) with the reference source at *f*in; the reference source also drives the DFS PLL.

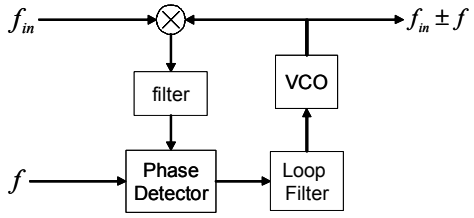

Figure 4. Diagram of offset synthesizer loop

We will use this approach to combine two DFS determined PLL to create a variable frequency synthesizer with a very small offset addition and subtraction (or net zero) from the *f*in reference. This structure can be cascaded k times to create any general k-order DFS PLL architectures.

C. Nested DFS Architecture(freq. offset)

As shown in Fig. 5, two DFS determined PLLs can be cascaded using the offset synthesizer structure to form a DFS architecture where the variable *f*out can be adjusted in very small resolution frequency steps from the fixed reference *f*in. Based on the DFS theorem 5.1 of [4], the PLL output frequencies of *f*1 and *f*2 can be determined by two mutually prime numbers N_1,N_2 and sectioned into fixed and variable parts where the variable part relates to the *a* of the Diophantine expression. More specifically, the numerator of each PLL 1 or 2 is split into a central fixed frequency determined by the integer pN_1 or pN_2 in a manner described for the constant c from [5]. The variable part of the numerator m_1 or m_2 is then allowed to take any value in the range of $-N_1,\ldots,N_1$ and $-N_2,\ldots,N_2$ respectively with the DFS advantage of allowing *a* to vary over the range $-N_1N_2,\ldots,N_1N_2$. Clearly under these conditions a setting of the variables exists where the net contribution to *f*out equals zero or *f*out = *f*in.

The additional fixed dividers Q and R are placed in the architecture to further refine the frequency resolution of the DFS architecture. The use of the dividers Q and R will slow the settling or transition time of the circuit but this parameter is not important to the scope of our demonstration synthesizer. As already noted, the same frequency resolution *f*in/QRN_1N_2 could be achieved by cascading one or two more DFS determined PLLs for fin/$N_1 \ldots N_k$, while recovering acquisition speed as each constituent PLL would settle at a time associate with a much smaller divider N_k.

Fig. 6 shows the numerical DFS design solution for our demonstration synthesizer. The solution shows the desired IF relationship of *f*1 and *f*2 at ~1 kHz and the 100 MHz reference to permit -100 dBc SPFD.

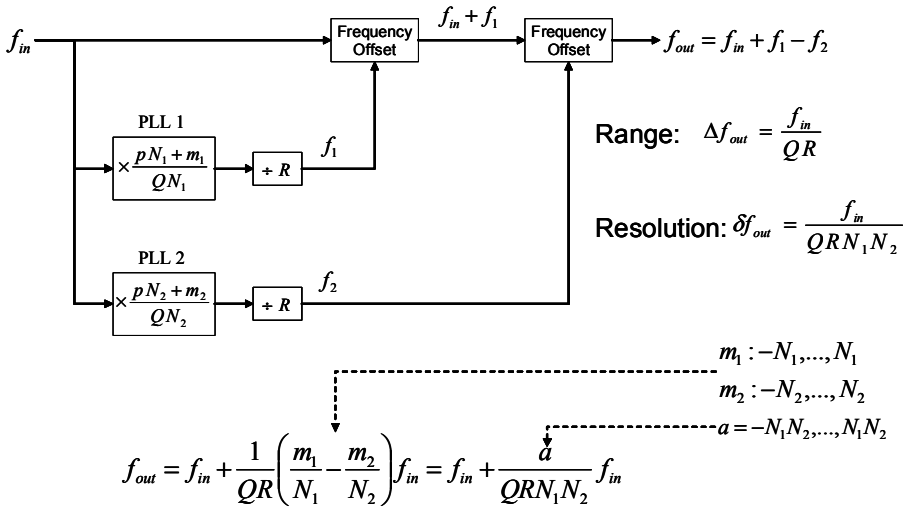

Figure 5. Diagram of two nested DFS determined PLL, k=2

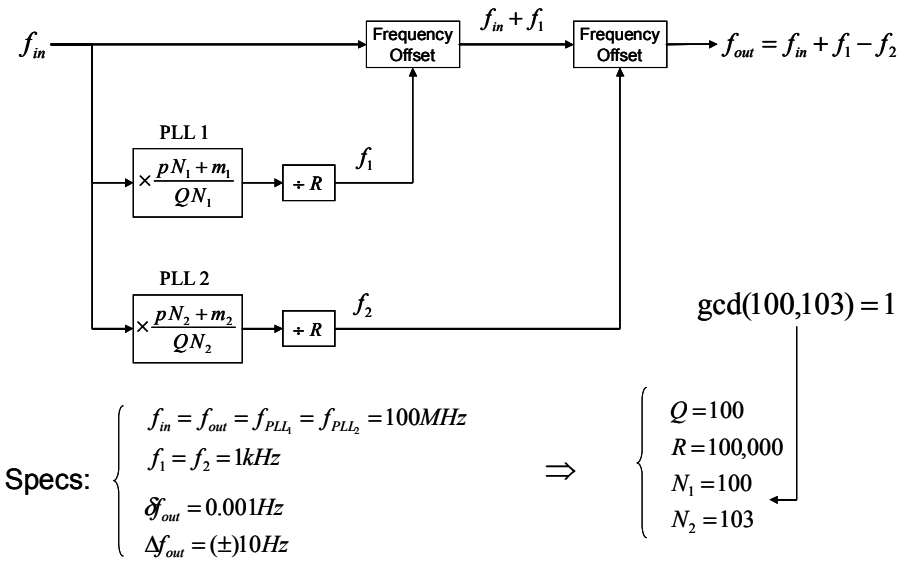

Figure 6. Numerical DFS solution for demonstration synthesizer

As described in Fig. 5, R was made large compared to Q, N_1 and N_2 to achieve the desired frequency step resolution of ± 0.001 Hz thereby keeping the PLL phase comparator frequencies large and easy to filter. This indicates our design emphasis on spectral purity over acquisition and our desire to achieve a practical circuit as simply as possible and not necessarily any fundamental constraint to the DFS method.

IV. Circuit Topology and Results from DFS Demonstration Synthesizer

Fig. 7 illustrates the complete block architecture of our DFS demonstration synthesizer. The theory of operation based on the previous sections uses two DFS determined PLLs driving two offset synthesizer architectures. The two VCXO's are chosen to be nominally *f*in with each having a control range of nominally ± (N_1*f*1)/*f*in or ±(N_2*f*2)/*f*in or approximately ±10 kHz. The first offset synthesizer generates a positive offset (*f*1 + *f*in), the second offset subtracts an offset (*f*2 + *f*in) to yield *f*out. DFS theory allows us to design the range of *f*1 and *f*2 to be practically similar to get zero offset or *f*in when they are equal and the full range of the synthesizer when both are at their maximal frequency values at either of their two polarity extremes. In this manner, the synthesizer generates very small offsets by adding the sum of the differences of f1 and f2 when they are close but not zero. The use of DFS theory also assures that the frequency step size will be uniform with the full variable range.

As stated previous, our desire was to build an expedient construction of the demonstration with the possibility of micro-circuit integration. This guided our choice for a substantial use of simple digital circuitry devices.

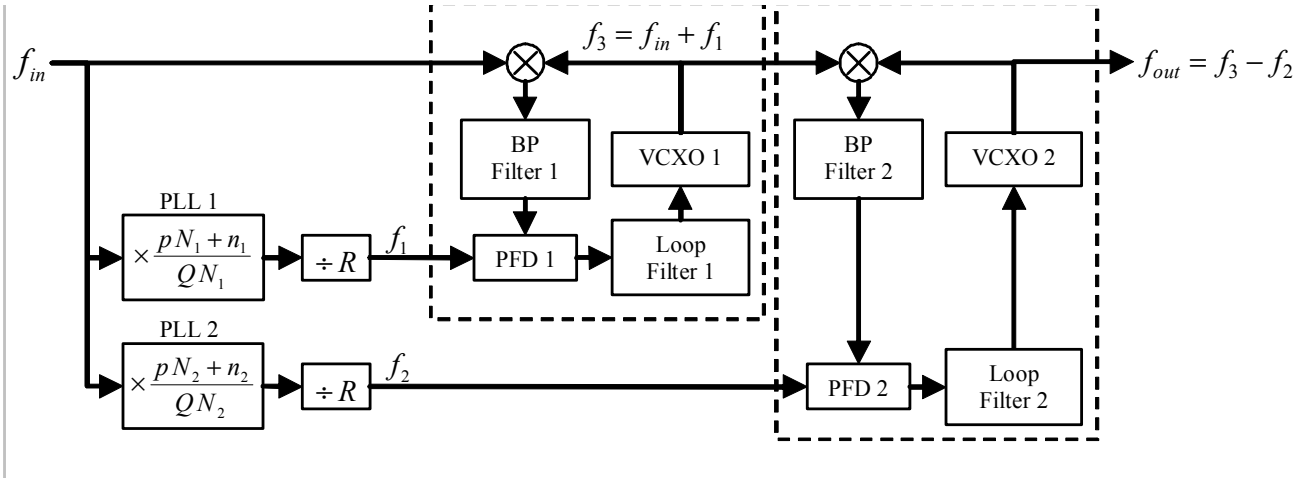

Figure 7. Block architecture of DFS demonstration synthesizer

For example, the frequency mixing is accomplished using an edge-triggered D-Flip-Flop technique. We have already discussed that this technique has the capability for a SFDR of -100 dBc at VHF *f*in (~100 MHz) by the ratio *f*1 / *f*in and *f*2 / (*f*in + (*f*1 – *f*2)) from Fig. 8. The two PFDs are standard charge-pump edge-triggered logic.

A. Mixer results

We chose the D flip-flop for mixing because of its simple, digital nature and requires no IF filtering. Although it is the least desirable of mixing methods for spurious level, its spurious performance is easily estimated by the ratio of IF/Fclk. Since the reference tones needed for the DFS demonstration could be accomplished around the 1 KHz region, we could still obtain an estimated worst case -100 dB spur level with this less than desirable method.

Another convenient property for the D flip-flop mixer is that the frequency offset of the two worst case (highest level) spurious $\pm S_1$ and $\pm S_2$ from the IF frequency can be determined within the range of 0 to 2×IF by the relationship,

$$\text{INT}\left[\frac{Fclk}{|IF|}\right] * |IF| - Fclk = S_1$$
$$\text{and if } S_1 < 0 \text{ then } S_2 = S_1 + |IF|$$
$$\text{otherwise } S_2 = S_1 - |IF| \qquad (9)$$

When we set the measurement equivalent to the frequency scheme for the demonstration synthesizer of a 1 KHz reference IF at a 100 MHz Fclk, we could not measure any spurious at their estimated locations above our system floor of -95 dBc in a resolution ~1 Hz BW.

Consequently, we performed a test using a higher IF/Fclk ratio (10kHz/10MHz) to confirm the spurious model at a measurable level. Fig. 8 shows the two pair of dominant tones in the 2×IF critical mixer performance bandwidth; ± 5734 and ± 4580. The frequency span of the measurement is 0 to 20 KHz, so the spurious shown represent the total number of spurs of interest over twice the reference tones of ~ 10 kHz.

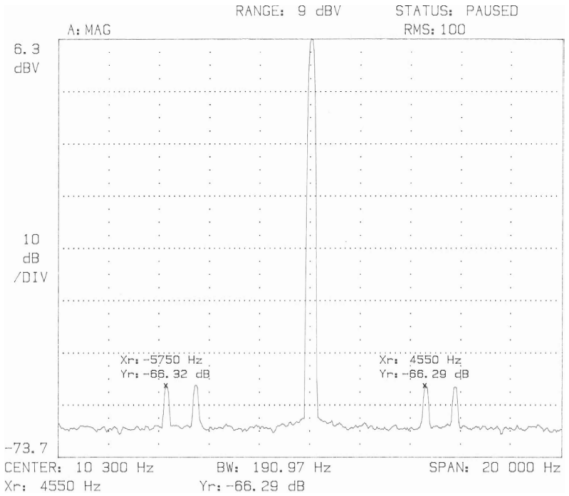

Figure 8. Measured spurious performance of D flip-flop test

The fact that the measured spurious in Fig. 8 was 6 dB better than the worst case estimation of -59 dBc at the frequencies located by the model provides confidence that our circuit implementation should meet the -100 dB goal.

B. Spectral Purity Results of Demonstration Synthesizer

The spectral purity measurement of a prototype of our DFS demonstration synthesizer is shown in Fig. 9. The output signal was measured at the first offset loop comparison, f3 (fin + f1) of Fig. 7 with the reference tone set to f1 equal to ~ 9.6 kHz. As measured, we show our synthesizer has a SPFD of better than -95 dBc over the frequency range of ± 25 kHz

This measurement span is greater than two times the reference tone on either side of the carrier and so should catch any of the unwanted spurious resultant from leakage of the mixer products or infiltration of the comparator reference through loop filter 1 of Fig. 7. We believe this measurement is the first, substantiated proof that the DFS

technique does provide for high spectral purity in fine frequency synthesis.

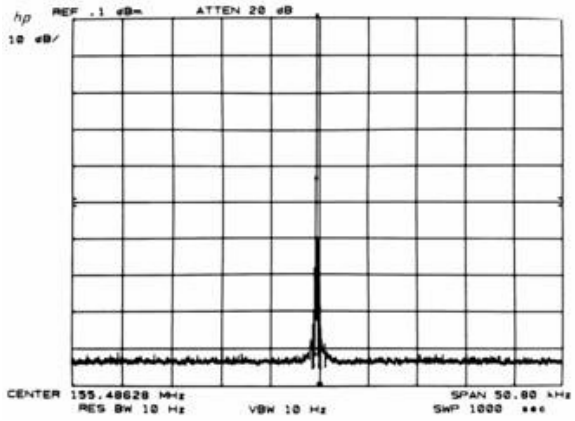

Figure 9. Spectrum measurement of DFS synthesizer

We note that throughout this paper, we describe a 100 MHz VHF synthesizer, but the availability of ± 100 ppm VCXO's made use of 155.52 MHz for our first prototype. This did not influence the design approach or topology other than scale the necessary DFS center frequencies which as we have made clear do not issue any significant restraint to the DFS technique.

V. SUMMARY

We continue to have great enthusiasm for the DFS method for synthesizer design. In summary, the general structure of DFS architectures provides the following desirable properties:

An ability to achieve a pre-determined center frequency, *f*out;

$$\bar{f}_{out} = \left(\frac{\overline{m}_1}{N_1} + \frac{\overline{m}_2}{N_2} + \ldots + \frac{\overline{m}_k}{N_k} \right) f_{in} \tag{10}$$

with a total variable frequency range of

$$\bar{f}_{out} - f_{in} \quad \text{to} \quad \bar{f}_{out} + f_{in} \tag{11}$$

and a frequency step resolution of

$$\frac{f_{in}}{N_1 N_2 \cdots N_k} \tag{12}$$

while maintaining the individual PLL comparator reference frequencies

$$\frac{f_{in}}{N_1}, \frac{f_{in}}{N_2}, \ldots, \frac{f_{in}}{N_k} \tag{13}$$

The application of DFS permits high flexibility on the relationship of the fixed frequency reference to output frequency (10) with wide variable range (11). Because of (12), very fine step size can be created from no more than four PLLs. Since the individual N_k prescalers of each constituent PLL can be kept small agile (fast settling time) frequency adjustment is not driven by step size and therefore optimized independently. Phase noise would be determined by the fin reference with spurious products are well controlled and easily filtered.

Our demonstration synthesized used the properties of DFS to optimize for the demanding requirements of high spectral purity and very small resolution steps. Other synthesizer requirements could also be approached given the flexibility of the DFS technique, for example fast frequency transition over large range

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